

In the Specification:

Please amend the specification as follows:

On Page 3, please replace the second paragraph with the following rewritten paragraph:

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The semiconductor wafer is placed on a test system and each integrated circuit chip is tested **215** for functionality. The functioning chips are denoted as functional die. The semiconductor wafer is then diced **220** and the functional die are separated for further assembly **225** in a first level or module package. The selection or omission of connections between the functional integrated circuit die and the first level package is a custom design particular to each combination of desired functions.

REMARKS

Examiner Peyton is thanked for the thorough examination of the subject Patent Application. The Claims have been carefully reviewed are considered to be in condition for allowance.

Reconsideration of the rejection under 35 USC §103(a) of Claims 1-51 as being unpatentable over applicants admitted prior art and U. S. Patent 6,054,767 (Chia et al.) is requested in light of the following argument.